IN THE CLAIMS:

Claims 45, 55, and 56 have been amended, as follows:

Claims 1 - 33 (cancelled).

34. (previously presented) A distributed memory switch system, comprising:

a plurality of ports including a source port and a destination port, wherein a packet is transmitted from the source port to the destination port;

a memory pool; and

an interconnection stage coupled between the plurality of ports and the memory pool such that the interconnection stage permits the packet to be sent from the source port to the destination port via the memory pool, the interconnection stage further splitting the packet received from the source port into a plurality of equal-sized packet portions for storage in the memory pool, wherein the interconnection stage includes a switch stage connected to the plurality of ports, and a memory switch connected to the switch stage and to the memory pool.

35. (previously presented) The distributed memory switch system of claim 34 wherein the switch stage includes a first set of ASICs connected to the plurality of ports.

36. (previously presented) The distributed memory switch system of claim 34 wherein the switch stage includes at least one ASIC connected to the plurality of ports.

37. (previously presented) The distributed memory switch system of claim 34 wherein the switch stage includes at least four ASICs connected to the plurality of ports.

38. (previously presented) The distributed memory switch system of claim 34 wherein the switch stage determines addresses in the memory pool for storing the packet received from the source port.

39. (previously presented) The distributed memory switch system of claim 34 wherein the interconnection stage reconstructs each of the plurality of equal-sized packet portions retrieved from the memory pool into the packet to be sent to the destination port.

40. (previously presented) The distributed memory switch system of claim 34 wherein the switch stage forms command signals which are associated with the packet received from the source port.

41. (previously presented) The distributed memory switch system of claim 34 wherein the memory switch includes a second set of ASICs connected to the switch stage and to the memory pool.

42. (previously presented) The distributed memory switch system of claim 34 wherein the memory switch includes at least four ASICs connected to the switch stage and to the memory pool.

43. (previously presented) The distributed memory switch system of claim 34 wherein the memory pool includes memory banks for respectively storing each of the plurality of equal-sized packet portions.

44. (previously presented) The distributed memory switch system of claim 34 further including:

a switch engine coupled to the interconnection stage for managing the flow of packets between source ports and destination ports.

45. (currently amended) The distributed memory switch system of claim 44 further ~~comprising~~ including:

a table RAM coupled to the switch engine, wherein the table RAM stores an

address corresponding to each of a plurality of temporarily stored packets.

46. (previously presented) A switch system for switching packets between ports, comprising:

an interconnection stage configured to transmit the packets between the ports; and

a memory pool coupled to the interconnection stage for storing the packets which are received from the ports, wherein the interconnection stage splits certain of the packets received from the ports into a plurality of equal-sized packet portions for storage in the memory pool, and the interconnection stage includes a switch stage connected to the ports and a memory switch connected to the switch stage and to the memory pool.

47. (previously presented) The switch system of claim 46 wherein the switch stage includes a first set of integrated circuits connected to the ports.

48. (previously presented) The switch system of claim 46 wherein the switch stage includes at least one integrated circuit connected to the ports.

49. (previously presented) The switch system of claim 46 wherein the switch stage includes at least four integrated circuits connected to the ports.

50. (previously presented) The memory switch system of claim 46 wherein the switch stage determines addresses in the memory pool for storing the packets received from the ports.

51. (previously presented) The switch system of claim 46 wherein the interconnection stage reconstructs the packet portions retrieved from the memory pool into the certain packet associated with the packet portions.

52. (previously presented) The switch system of claim 46 wherein the switch stage forms command signals which are associated with certain of the packets received from the ports.

53. (previously presented) The switch system of claim 46 wherein the memory switch includes a second set of integrated circuits connected to the switch stage and to the memory pool.

54. (previously presented) The switch system of claim 46 wherein the memory switch includes at least four integrated circuits connected to the switch stage and to the memory pool.

55. (currently amended) The switch system of claim 46 further ~~comprising~~ including:

a switch engine coupled to the interconnection stage for managing the flow of the packets between the ports.

56. (currently amended) The switch system of claim 55 further ~~comprising~~ including:

a table RAM coupled to the switch engine, wherein the table RAM stores an address corresponding to each of a plurality of temporarily stored packets..

57. (previously presented) The switch system of claim 46 wherein the memory pool is comprised of memory banks for respectively storing the plurality of equal-sized packet portions.